

# Phillips Scientific

## 16 Channel Individual Gate Charge ADC

### CAMAC MODEL 7167 7167H

### FEATURES

- \* The Model 7167 Features LEMO Inputs
- \* The Model 7167H has Differential Header Inputs
- \* Individual GATE and CHARGE Inputs for Each Channel
- \* Less Than 7.2  $\mu$ Sec Conversion and Processing Time
- \* 12-Bit Dynamic Range, Resolution to 125 fC/Count
- \* Programmable Pedestal Correction
- \* Sparse Data Scan with Lower and Upper Threshold Cuts
- \* Fast CLEAR and COMMON ENABLE Window
- \* Built-in Test Features Check QDC and Digitization

### DESCRIPTION

The Model 7167/H QDC implements 16 channels of Charge to Digital Conversion (QDC), each with its own GATE, followed by a digital processing section and CAMAC interface in a double width CAMAC module. To minimize data readout time, the QDC performs a sparse data function. Channels can be individually programmed with pedestal correction and both lower and upper level thresholds. Digitization starts following release of the COMMON ENABLE input. It may be delayed by a user-programmable amount to allow time for derivation of fast CLEAR signals.

Channels that meet the sparsification requirements will have corresponding bits set in the Hit Register. Subsequent events will be ignored until the Hit Register is cleared either by completing a sparse read of the module or via front panel FAST CLEAR or CAMAC Clear commands.

### CHARGE INPUTS

#### Input Impedance

**Single Ended** : 51 ohm,  $\pm 2\%$ , direct coupled. (AC coupling optional).

**Differential** : 102 ohm,  $\pm 2\%$ , direct coupled. (AC coupling optional).

**Voltage Compliance** : 0 to -2.5 Volts; **Common Mode**:  $\pm 2.5$  Volts DC.

#### Input Offset

**Single Ended** : 0 to 2mVolt, (40 $\mu$ Amp) maximum.

**Differential** : 0 to 2mVolt, (20 $\mu$ Amp) maximum.

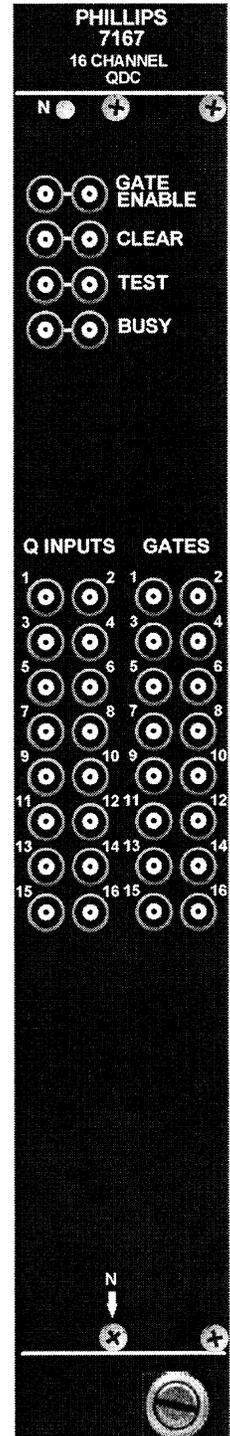
**Dynamic Range** : -512pC full scale, -125fC/Count  $\pm 2\%$ , 12-bit Range.  
(Other ranges available).

**Charge Feedthrough** : Less than  $\pm 0.1\%$  of input.

**Internal Signal Coupling** : Front-end is AC coupled to the current integration stage with a 3.3 mSec time constant. Other time constants or DC coupling is available. **Note:** When direct-coupled, small input offset voltages can cause large pedestals.

**Stability** : Better than 5fC/  $^{\circ}$ C between 0  $^{\circ}$ C to 60  $^{\circ}$ C.

**Pedestal vs. Gate Width** : Less than 40fC/nSec.



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## **CLEAR, GATE and TEST INPUTS**

**LEMO Inputs (7167)** : NIM logic levels; Two LEMO connectors per input to facilitate daisy chaining. Input impedance 5.1K ohm; 50 ohm terminate at last module in chain.

**ECL Inputs (7167H)** : Differential ECL logic levels; 2 pairs per input to facilitate daisy chaining; Terminate at end of chain with 110 ohms.

**GATE ENABLE Input** : Common to all channels, enables the individual gate inputs. Processing of events begins at end of enable pulse. Usable from 50nSec to 10 $\mu$ Sec. Must extend at least 10nSec before and after all individual gates.

**Individual Gates** : 20nSec to 10 $\mu$ Sec; should precede the charge input by 20nSec minimum; no charge dependence on position of analog event within gate, other than pedestal vs. gate effect. **Note:** When operating with GATE durations greater than several microseconds, large pedestals can be present due to the integration of small input signals or levels;  $Q$  (Charge) =  $I$  (Current) x  $T$  (Time)

**GATE Feedthrough** : Less than  $\pm 0.5$  pC.

**CLEAR Input** : Common to all channels, accepts 10nSec or greater input width.

**CLEAR Settling time** : Less than 750nSec to within one count.

**CLEAR Function** : Halts conversion, locks out any new gate, clears analog data, most recent digital data and hit register.

**TEST Input** : Leading edge causes a GATE and analog input to be applied to all channels. Digitizes to approximately 1/4 full scale calibration. NOT intended for precise calibration of the module.

### **BUSY Output**

**LEMO (7167)** : Two paralleled LEMO connectors, bridged negative NIM logic 32mA.

**ECL (7167H)** : Two double row connector pins; Differential ECL logic output.

Active from the trailing edge of GATE ENABLE until the event has been aborted by CLEAR or has been fully digitized and read out through the sparse data port. BUSY follows the Hit Register and thus may also be released by clearing the Hit Register. Useful for minimizing QDC dead time when folded into the fast trigger logic.

## **FRONT END PERFORMANCE**

A dithered mode may be selected by the user for improved performance in spectroscopy analysis. It should be disabled when working within the bottom or top 1.5% of the module's range or for those measurements not creating histograms of data

**Linearity** : Integral : Less than 3 counts over 10% to 90% of range.  
Differential : Less than 0.025% of full scale maximum.  
Non-Dithered :  $\pm 0.5$  bins typically.  
Dithered :  $\pm 0.1$  bins typically.

**Crosstalk** : 1 LSB maximum between adjacent channels operated within range.

**Conversion Time** : 7.2 $\mu$ Sec maximum, includes 750nSec for settling and for accepting fast CLEAR signals. Timing is measured from the trailing edge of the COMMON ENABLE signal. Digitization may be delayed by 0 to 16 $\mu$ Sec in 62.5nSec increments with external jumpers. The increased delay may be used to allow a greater acceptance window for CLEAR signals.

**Power Supply Requirements** : + 6V @ 2.6 Amps typically  
- 6V @ 2.0 Amps typically  
+24V @ 400 mA typically  
Forced air cooling is recommended.

## **ADDITIONAL TEST FEATURES**

- Calibration Check** : Simulates a Charge/Gate sequence under CAMAC control to verify operation of the module. CAMAC selectable nominal 1/3 or 2/3 full scale calibration. Not intended for precise calibration of the module.
- CAMAC Check** : Loads a predetermined pattern to simulate the outputs of the A/D converters. Useful for verifying the operation of the processing sections of the module.

## **SPARSIFICATION and LAM OPERATION**

Separate pedestals and upper and lower thresholds may be set for each channel. They are enabled using bits in the Control Register. Pedestals in signed 2's complement format are added to the data before threshold comparison. Bits in the Hit Register are set during digitization for those channels whose pedestal corrected data falls within their upper and lower thresholds. If enabled, LAM is set whenever a bit in the Hit Register is set. Sparse data reads present only those channels with bits set in the Hit Register, starting with the highest numbered channel. As channels are read, their Hit Register bits are reset; when the final channel has been read LAM is reset. LAM is also reset when the Hit Register is reset.

## **DATA WORD FORMAT**

16	13	12	1
Channel ID		Channel Data	

## **CONTROL REGISTER FORMAT**

16	9	8	4	3	2	1
Conversion Delay (Read Only)		0	UT Enable	LT Enable	PED Enable	

## **CAMAC DATAWAY OPERATIONS**

- F(0)·A(X)** : Read event data memory for Channel (X+1). Data word as described above.
- F(1)·A(X)** : Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).
- F(4)·A(0)** : Read Sparse Data. Only those channels with data that falls between their upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false. Data word as described above.
- F(6)·A(0)** : Read the Control Register. Format described above.
- F(6)·A(1)** : Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds.
- F(8)** : Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.
- F(9)** : Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

## **CAMAC DATAWAY OPERATIONS** (continued)

- F(10)** : Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.
- F(11)·A(0)** : Reset the Control Register. Occurs on S2 strobe.
- F(11)·A(1)** : Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.
- F(11)·A(2)** : Reset the Test Register. Occurs on S2 strobe.
- F(11)·A(3)** : Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.
- F(16)·A(X)** : Write to data memory for channel (X+1).
- F(17)·A(0)** : Select the Pedestal Memory for the next F1 or F20 operation.
- F(17)·A(1)** : Select the Lower Threshold Memory for the next F1 or F20 operation.
- F(17)·A(2)** : Select the Upper Threshold Memory for the next F1 or F20 operation.
- F(17)·A(4)** : Select the Test Register for the next F20 operation.
- F(19)·A(0)** : Set the Control Register bits. Format described above.
- F(20)·A(X)** : Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation. Pedestal range is  $\pm 4095$ ; threshold ranges are 0 to 4095. Program the test register if it was selected by the most recent F17 operation.
- A0 : Test pattern = 001001001001  
A1 : Test pattern = 010010010010  
A2 : Test pattern = 100100100100  
A3 : Test pattern = 111111111111
- F(23)·A(0)** : Reset the Control Register bits. Format described above.
- F(24)** : Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.
- F(25)·A0** : Digital test. Initiates a data acquisition cycle using the value stored in the Test Register by the most recent F20 command.
- F(25)·A1** : Test. Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.
- F(25)·A2** : Test. Runs a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.
- F(26)** : Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.
- C, Z** : Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.
- I** : Inhibits QDC Front End.