

### FEATURES

- \* 7132 Features NIM/TTL with LEMO's, 7132H Differential ECL Header Inputs
- \* 32 Scalers, 24-Bits long or 16 Scalers, 48-Bits long
- \* Scalers may be Read Out or Preset Individually or in Q Block Mode
- \* Fast Clear and Inhibit Inputs
- \* LAM on Overflow on Any Scaler
- \* Programmable Inhibit on Overflow
- \* Done Output on Overflow
- \* Built-in Test Features

### DESCRIPTION

The Model 7132/7132H scaler implements thirty-two scalers, 24-bits long, or sixteen scalers, 48-bits long in a single width CAMAC module. The high density, versatility and 225 MHz count rate are unmatched. Each scaler consists of a presettable up counter with NIM/TTL or differential ECL inputs. Clear, Inhibit and Test inputs are common to all 32 scalers. When any counter overflows, LAM and/or Done may be generated. When Inhibit on Overflow is enabled, a channel may be programmed to inhibit itself and other channels from counting. Any counter may be preset with the 1's complement of a desired count; this configures it as a programmable countdown scaler or programmable timer function.

### FRONT PANEL INPUTS

**Lemo Inputs (7132)** : Accepts positive TTL and negative NIM level signals. TTL threshold typically +1.2Volts; NIM threshold typically -500mVolt.

**NIM** : Input impedance 50 ohm,  $\pm 10\%$ ; Inputs protected to  $\pm 8VDC$ .

**TTL** : Input impedance 1000 ohm,  $\pm 10\%$ ; Inputs protected to  $\pm 8VDC$ .

**Bridged NIM Inputs** : Available as an option on control inputs; (Clear, Inhibit and Test). Useful for daisy-chaining multiple 7132 modules; Input impedance 1K ohm; Will not respond to TTL level inputs. Specify when ordering.

**ECL Inputs (7132H)** : Two dual row x 17 pin headers; Accepts differential ECL inputs; 200mVolt threshold. Removable 110 ohm input termination.

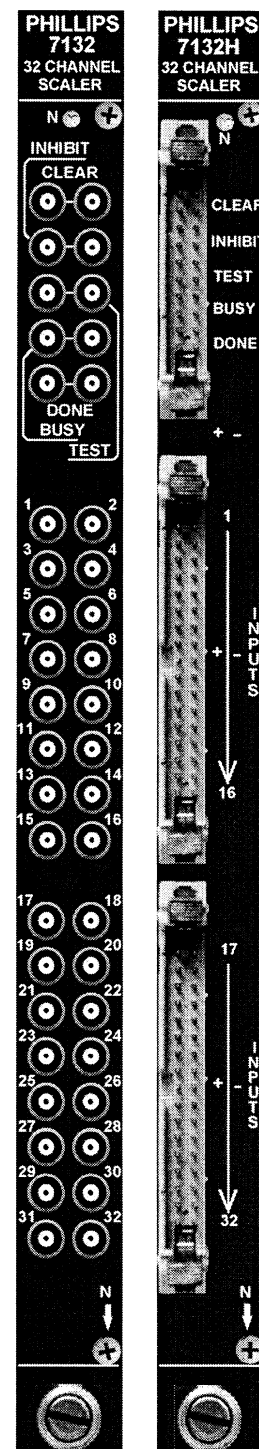
**Input Channel 1 to 32** : Clock inputs to scalers normally configured as 32, 24-bit scalers. When configured as sixteen 48-bit scalers, the inputs are fed to the odd numbered channels. Minimum input pulse width 2.0nSec.

**Count Rate** : NIM/ ECL : Greater than 225 MHz.  
TTL : Greater than 50 MHz.

**Fast Clear** : Clears all scalers; May be applied at any time. Minimum input width 20nSec. Requires 30nSec for next scaler Clock input to be recognized after the trailing-edge of Clear input.

**Inhibit Input** : Inhibits all scalers from counting inputs within 1.5nSec. Minimum input width is 4nSec. Allow 20nSec after Inhibit trailing-edge to recognize the next scaler Clock input. Will not inhibit counting of CAMAC initiated test counts or front panel test inputs.

**Test Function** : Common to all channels; Used to clock all scalers when the module is inhibited by CAMAC I or the front panel Inhibit. Minimum pulse width 5nSec; Maximum frequency 100MHz.



## FRONT PANEL OUTPUTS

- 7132** : LEMO output connectors; NIM current-switching bridged outputs -32mA, (-1.6Volts into a single 50 ohm load and -800mV into two 50 ohm loads).
- 7132H** : Differential ECL header outputs. Capable of driving two 110 ohm loads.
- DONE Output** : Pulsed on overflow for those channels selected by the Done On Overflow Register. Latency time from clock to Done Output is 100nSec typical; Pulse width 64nSec min. to 96nSec max.
- BUSY Output** : Active when the module is inhibited from the front panel Inhibit or from CAMAC and during any CAMAC operation. When the Configuration Register is written to or reset, Busy will be active for up to 300 mSec.

## TEST FEATURES

- Front Check** **End** : All scalers are clocked with the front panel Test input. The module must be inhibited from the front panel Inhibit or from CAMAC. This ensures that the scaler inputs are not being clocked by external events during a test sequence.
- CAMAC Check** : A programmed number of 32 MHz clocks equal to the number stored in the Test Count Register is applied to all channels. The module must be inhibited from the front panel Inhibit or from CAMAC Inhibit to lock out any external events during a test sequence.

## GENERAL PERFORMANCE

- Power Supply Requirements** : +6 Volt @ 1.4 Amps typical; } Forced air cooling is recommended when operating  
- 6 Volt @ 2.5 Amps typical; } adjacent modules in a crate.
- Operating Temp.** : 0 °C to 60 °C ambient.
- Packaging** : Standard single width CAMAC module in accordance with ESONE Report EUR 4100.

## PROGRAMMING REGISTERS

### SCALER BANK SELECTION REGISTER :

Contains the bank of scalers for the next CAMAC command as well as the address and bank of scalers for the next sequential access commands (F4 or F20) as follows:

D24	D10	D9	D5	D4	D2	D1
Not Used		SA4 Sequential Address	SA0	Not Used		Scaler Bank

D1: Selects scaler bank; D1 = 0 accesses channels 1 to 16, D1 =1 accesses channels 17 to 32.  
D5-D9: Sequential access address, SA [4..0]; Points to the address that the next CAMAC cycle will execute.

### TEST COUNT LENGTH REGISTER :

Sets the number of 32 MHz pulses applied to all scalers at the test command. Up to 255 pulses may be programmed, using D [8..1].

### LAM MASK REGISTER :

Allows LAM to be generated on overflow on selected channels when LAM is enabled. Bits set to 1 allow LAM on overflow for their corresponding channels. Addressing is same as the Inhibit On Overflow Register.

### LAM STATUS REGISTER :

Read only; Bits set to 1 indicate overflow for the corresponding channel. This register is 'AND'ed with the Inhibit on Overflow Register to produce Inhibit on Overflow and with the LAM Mask Register to produce LAM when LAM is enabled. Addressing is same as the Inhibit on Overflow Register.

### DONE ON OVERFLOW REGISTER :

Enables The Front Panel Done output for each channel in the 7132/7132H. Bits set to 1 enable Done on Overflow for their corresponding channels. Addressing is same as the Inhibit on Overflow Register.

## PROGRAMMING REGISTERS (continued)

### INHIBIT ON OVERFLOW REGISTER :

Enables inhibit on overflow for selected channels as described in Tables 1 and 2. When Scaler bank 0 is selected (Scalers 1 to 16) each bit enables the corresponding channel. With Scaler bank 1 selected (Scalers 17 to 32), each bit enables the corresponding channel + 16 (bit 1 enables channel 17 and so on). Bits set to 1 enable Inhibit on Overflow for their corresponding channels.

### INHIBIT ON OVERFLOW OPERATION :

There are four inhibit on overflow modes, as described below. Inhibit on overflow mode is controlled by setting the appropriate bits in the Control Register. Input to Inhibit on Overflow time (any channel, any configuration): Less than 95nSec.

**TABLE 1: THIRTY-TWO 24-BIT SCALERS**

Overflow on Channel	Inhibits Channels			
	Mode 0	Mode 1	Mode 2	Mode 3
1	1,2	1-4	1-8	1-16
2	-	-	-	-
3	3,4	-	-	-
4	-	-	-	-
5	5,6	5-8	-	-
6	-	-	-	-
7	7,8	-	-	-
8	-	-	-	-
9	9,10	9-12	9-16	-
10	-	-	-	-
11	11,12	-	-	-
12	-	-	-	-
13	13,14	14-16	-	-
14	-	-	-	-
15	15,16	-	-	-
16	-	-	-	-

Overflow on Channel	Inhibits Channels			
	Mode 0	Mode 1	Mode 2	Mode 3
17	17,18	17-20	17-24	17-32
18	-	-	-	-
19	19,20	-	-	-
20	-	-	-	-
21	21,22	21-24	-	-
22	-	-	-	-
23	23,24	-	-	-
24	-	-	-	-
25	25,26	25-28	25-32	-
26	-	-	-	-
27	27,28	-	-	-
28	-	-	-	-
29	29,30	29-32	-	-
30	-	-	-	-
31	31,32	-	-	-
32	-	-	-	-

**TABLE 2: SIXTEEN 48-BIT SCALERS**

Overflow on Channel	Inhibits Channels			
	Mode 0	Mode 1	Mode 2	Mode 3
1	1	1,3	1-7	1-15
3	3	-	-	-
5	5	5,7	-	-
7	7	-	-	-
9	9	9,11	9-15	-
11	11	-	-	-
13	13	13,15	-	-
15	15	-	-	-

Overflow on Channel	Inhibits Channels			
	Mode 0	Mode 1	Mode 2	Mode 3
17	17	17,19	17-23	17-31
19	19	-	-	-
21	21	21,23	-	-
23	23	-	-	-
25	25	25,27	25-31	-
27	27	-	-	-
29	29	29,31	-	-
31	31	-	-	-

### CONFIGURATION REGISTER FORMAT :

D24	D7	D6	D5	D4	D2	D1
Not Used		Inhibit on Overflow Mode			Not Used	Configuration
		D6	D5	Mode	(Default)	0 Selects 32 24 Bit Scalers (Default)
		0	0	0		1 Selects 16 48 Bit Scalers
		0	1	1		
		1	0	2		
		1	1	3		

## **CAMAC DATAWAY OPERATIONS**

- F(0)•A(X)** : 32-Bit Mode: Read scaler (X+1) in the bank selected by the Scaler Bank Selection Register.  
48-Bit Mode: Even addresses read the lower 24 bits and odd addresses read the upper 24 bits of a scaler in the bank selected by the Scaler Bank Selection Register.
- F(1)•A(0)** : Read the Configuration Register.  
**F(1)•A(1)** : Read the Scaler Bank Selection Register.  
**F(1)•A(2)** : Read the Test Count length.  
**F(1)•A(3)** : Read the Inhibit on Overflow Register for the bank selected by the Scaler Bank Selection Register.  
**F(1)•A(5)** : Read the Done on Overflow Register for the bank selected by the Scaler Bank Selection Register.  
**F(1)•A(12)** : Read the LAM Status Register for the bank selected by Scaler Bank Selection Register.  
**F(1)•A(13)** : Read the LAM Mask Register for the bank selected by the Scaler Bank Selection Register.  
**F(2)•A(X)** : Read and Reset Scaler and LAM. See F(0)•A(X) for addressing.  
**F(4)•A(15)** : Q Block read. Sequentially reads scalers starting at address in Scaler Bank Selection Register. After accessing scaler 32, the next command will return Q =0. The Scaler Bank Selection Register must be reprogrammed to reuse this command.
- F(8)** : Test LAM. A Q =1 response is generated if LAM is present and enabled. The address lines have no effect on this command.
- F(9)•A(X)** : Reset Scaler and LAM. See F(0)•A(X) for addressing.  
**F(10)•A(X)** : Reset LAM. See F(0)•A(X) for addressing. Channels which have been inhibited by overflow on the addressed scaler are enabled.
- F(11)•A(0)** : Clear the Configuration Register. Also clears Inhibit on Overflow Register, LAM Mask, Done on Overflow Register and LAM Status Register. This command requires about 300 mSec to complete operation. Occurs on S2 strobe.  
**F(11)•A(1)** : Reset the Scaler Bank Selection Register. Occurs on S2 strobe.  
**F(11)•A(2)** : Reset the Test Count Length Register. Occurs on S2 strobe.  
**F(11)•A(3)** : Reset Inhibit on Overflow Register. Enables all channels inhibited by overflow. Occurs on S2 strobe.  
**F(11)•A(4)** : Reset all scalers, and LAM. Enables all channels inhibited by overflow. Occurs on S2 strobe.  
**F(11)•A(5)** : Reset Done on Overflow Register. Occurs on S2 strobe.  
**F(11)•A(12)** : Reset the LAM Status Register. Enables all scalers inhibited by overflow. Resets all LAMs. Occurs on S2 strobe.  
**F(11)•A(13)** : Reset the LAM Mask Register. Occurs on S2 strobe.
- F(16)•A(X)** : Load Scaler. See F(0)•A(X) for addressing. Resets the LAM Status Bit for Scaler on S2 strobe. Any channels previously inhibited by overflow on channel (X+1) will be enabled by the S2 strobe.
- F(17)•A(0)** : Program the Configuration Register. See F(11)•A(0).  
**F(17)•A(1)** : Write to the Scaler Bank Selection Register.  
**F(17)•A(2)** : Write to the Test Count Length Register.  
**F(17)•A(3)** : Write the Inhibit on Overflow Register.  
**F(17)•A(5)** : Write the Done on Overflow Register.  
**F(17)•A(13)** : Write the LAM Mask Register for the bank selected.
- F(20)** : Q Block Load. Sequentially loads scalers. See F(4) for addressing.  
**F(24)** : Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.
- F(25)•A(0)** : Enables the test clock for the number of counts programmed into the Test Count Length. The module must be inhibited from Front Panel Inhibit or CAMAC I for clocks to be generated.
- F(26)** : Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.
- Z** : Reset all Scalars and LAM's. Enables all Scalars inhibited by overflow. Reset all registers. This command requires about 300 mSec to complete operation.
- C** : Reset all Scalars and LAM's. Enables all Scalars inhibited by overflow. Resets the Scaler Bank Selection Register to 0.
- I** : Inhibit the Scalars from counting normal input pulses. Allow test pulses from the front end or internally by CAMAC commands.

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